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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,546	01/16/2002	Jerry D. Hayes	BUR920000201	7715

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EXAMINER	
THOMPSON, ANNETTE M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,546	HAYES, JERRY D.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-21,24-27 and 30* is/are rejected.

7)☒ Claim(s) *3,22,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Amendment under 37 CFR 1.116 has been examined and entered. However, this application is not in a condition for allowance and after further consideration, this second non-final action on the merits is issued with new grounds of rejection.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 6, 7, 8, 11, 15, 17, 18, 24-27 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Pursuant to claims 4 and 15, the claim limitation "where the characterization of the switching elements as of the voltage-time controlled resistors is started with a midpoint of the input transition" is confusing; Applicant's disclosure at page 6, paragraph [0037] states "The transient impedance of the NFET *turning on* is a function of device voltage and of "local time" that *begins at the midpoint of the input transition.* Pursuant to claims 6 and 17 Applicant's limitation does not properly claim the invention, i.e. according to Applicant's specification [¶ 0038] it is the time indexing of the scalars which are controlled; examiner suggests rephrasing of the limitation starting at line 3 "time as a function of periodic rising and falling input edge arrival time"; delete or correct "controlling time through indexing equations" based on Applicant's specification [¶ 0038]. Pursuant to claims 7 and 18, Applicant's specification [¶ 0060] states that it is the K1-K12

modulators that account for variations in environmental conditions. Pursuant to claims 11 and 24-27, Applicants fail to properly claim the invention as specified in Applicant's specification at [¶ 0093]. Claims dependent from rejected base claims are likewise rejected.

Claim Objections

3. Claim 29 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 28. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

4. Claims 3, 4, 11, 12 and 22, 28 and 29 are objected to because of the following informalities: Pursuant to claim 3, at line 3, change "dc" to - -DC- -. Pursuant to claims 11 and 22, at line 1, delete "where the method". Pursuant to claims 3 and 12, change "dc" to - -DC- -. Pursuant to claim 4, before "voltage", delete "of the". Pursuant to claim 28 and 29, at lines 12 and 11, respectively, "affects" should be - -effects- -. Appropriate correction is required.

5. Additionally, claims 1, 3, 4, are objected to because of the following informalities: Pursuant to claims 1, 12 and 28, at line 8, after "elements", insert - -represented- -. Pursuant to claim 3, at line 2, delete "as voltage time-controlled resistors". Pursuant to claims 4 and 15, the claim limitation "where the characterization of the switching elements as of the voltage-time controlled resistors is started with a midpoint of the input transition" is confusing based on Applicant's disclosure. Pursuant to claim 24, it

depends from a cancelled claim. Pursuant to claims 1, 13, 28 and 29, after the first occurrence of dc_base, insert - -impedance- -. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5, 9, 10, 12, 16, 20, 21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over The IBIS specification, version 3.2, ANSI/EIA-656-A, ratified August 1999, in view of the Wang et al. paper entitled The Development of Analog SPICE Behavioral Model Based on IBIS Model. The IBIS specification discloses a method for modeling IO however it does not explicitly discloses characterizing the switching elements as voltage time controlled elements. The Wang paper at least suggests, if not discloses, some of the working details of the IBIS specification and it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to rely on the details of the Wang paper for some additional clarification of the IBIS method.

8. Pursuant to claims 1, 12 which recites a method for creating a model of inputs and outputs of integrated circuits (the IBIS specification), comprising the steps of representing in the model the output characteristics of integrated driver circuits by two types of elements, switching and non-switching (Wang, §§ 2, 2.1 discloses transistors and power clamping diodes); tabulating the output characteristics for each of the

elements by applying a DC voltage source on the output of the driver circuits and measuring the current through each element (Wang, § 2 references DC IV tables) ; characterizing the switching elements as voltage-time controlled resistors (§ 2.1 references pullup and pull down transistors) by obtaining the product of DC impedance (conductance) as a function of voltage and scalars that are functions of time (Wang, §§ 2, 2.2) ; and embedding in the model, equations that are functions of input edge arrival times and cycle time for each scalar (Wang, §§ 2.2 and 2.3).

9. Pursuant to claims 5 and 16 further comprising the step of saving the scalars in a tabular format (§ 2.2, Ku(t) and Kd(t) and § 2.3, multipliers Kx(t)).

10. Pursuant to claims 9 and 20, wherein the switching elements reflect composite transient impedance behavior of a pull-up or pull down network that are comprised of a plurality of FETs and parasitics (§ 2.1).

11. Pursuant to claims 10 and 21, wherein the non-switching elements are an ESD device and a power clamp (§ 2.1, ¶ 1).

12. Pursuant to claim 30, which recites a program storage device readable by a machine, tangibly embodying a program of instructions executable by a machine, to perform method steps for creating a model of inputs and outputs of integrated circuits (Wang, § 1 wherein IBIS is an EDA based tool and EDA tools inherently utilize program storage devices); representing in the model the output characteristics of integrated driver circuits by two types of elements, switching and non-switching (Wang, §§ 2, 2.1 discloses transistors and power clamping diodes); tabulating the output characteristics for each of the elements by applying a DC voltage source on the output of the driver

circuits and measuring the current through each element (Wang, § 2 references DC IV tables) ; characterizing the switching elements as voltage-time controlled resistors (§ 2.1 references pullup and pull down transistors) by obtaining the product of DC impedance (conductance) as a function of voltage and scalars that are functions of time (Wang, §§ 2, 2.2) ; and embedding in the model, equations that are functions of input edge arrival times and cycle time for each scalar (Wang, §§ 2.2 and 2.3).

Allowable Subject Matter

13. The following is a statement of reasons for the indication of allowable subject matter: In a method for creating a model of inputs and outputs of integrated circuits, the prior art does not teach or suggest accounting for variations in temperature and supply voltages wherein the characteristics for the switching and non-switching elements are obtained from the equation dc_impedance = (1+D0)*dc_base.

Conclusion

14. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

15. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

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